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Urgent

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Date: February 25, 2005

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Examiner David A. Zarneke USPTO	(703) 872-9306	2829

From:	Fax:	M/S:
B. Delano Jordan	301-474-2270	

Subject: Electrical/Optical Integration Scheme Using Direct Copper Bonding
Application No.: 10/020,911; Inventor: Gilroy J. Vandentop, et al.
Filed: December 19, 2001 Docket No. P12665

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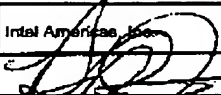
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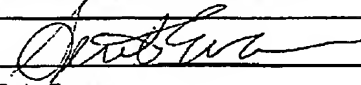
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	Filing Date	December 18, 2001
	First Named Inventor	Gilroy J. Vandenberg
	Art Unit	2829
	Examiner Name	David A. ZARNEKE
	Attorney Docket Number	P12686
Total Number of Pages in This Submission		6

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Firm Name	Intel America, Inc.		
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Printed name	B. Delano Jordan		
Date	2/25/05	Reg. No.	43,698

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P12665

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gilroy J. Vandentop, et al.

Serial No.: 10/020,911

Filing Date: December 19, 2001

For: ELECTRICAL/OPTICAL
INTEGRATION SCHEME USING
DIRECT COPPER BONDING

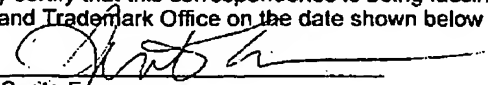
Examiner: Zarneke, David A.

Art Unit: 2829

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O Box 1450
Alexandria, VA 22313-1450REPLY BRIEF UNDER 37 C.F.R. § 41.41

Dear Sir:

Appellants hereby submit this Brief in response to the Examiner's Answer mailed on December 27, 2004 in the above-referenced application. Appellants respectfully request consideration of this Reply Brief by the Board of Patent Appeals and Interferences, and for allowance of the above-referenced application.

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Electro-optic intermediate wafers are not admitted prior art

Claim 1 recites "providing an intermediate wafer having one or more intermediate contact pads... connected to an *electro-optic* arrangement on the intermediate wafer" (emphasis added).

The Examiner's Answer states, "Applicant's admitted prior art teaches... an intermediate wafer having one or more intermediate contact pads... connected to an electro-optic arrangement on the intermediate wafer" (Examiner's Answer, pg. 3). As far as Appellants can discern, the Examiner appears to be relying on two sentences in the background discussion section of the Specification:

- 1) "While optical losses could be avoided to some degree by placing the optical detector on the intermediate wafer [i.e., fabricate an electro-optic intermediate wafer], it has been determined that C4 bonding can also present problems from an electrical standpoint." (Specification, para. [0005], lines 9-10, emphasis added); and
- 2) "Thus, manufacturers and designers of conventional electro-optic semiconductor packages are faced with the difficult choice between the optical losses associated with IC wafer placement of the optical detector [i.e., optical intermediate wafer] and the electrical losses associated with intermediate wafer placement of the optical detector [i.e., electro-optic intermediate wafer]." (Id., lines 13-16, emphasis added).

Appellants assert, however, that as a whole, the Specification establishes that before the claimed invention, the conventional approach was to fabricate a purely optical intermediate wafer by positioning the optical detector on the IC wafer. Indeed, the specification explicitly states that "[c]onventional semiconductor packages that make use of optics often provide an IC wafer and an intermediate wafer that has an optical arrangement" (Specification, para. [0004], lines 4-6). The specification goes on to explain that "[t]he optical arrangement will typically include a waveguide and a coupler such as a Bragg grating" (Id., lines 6-7) and that "it is common to provide a photo detector on the IC wafer that is aligned with the optical coupler during the fabrication process" (Id., lines 11-12). Thus, it is clear from the Specification that conventional intermediate wafers had a purely optical arrangement before the claimed invention was made.

Because Fan also fails to disclose intermediate wafers with electro-optic arrangements, all of the claimed limitations are not taught or suggested by the references and a prima facie case of obviousness has not been met. For at least the above reasons, claims 1-4, 14-16 and 31 recite patentable subject matter. Accordingly, Appellants request that the Examiner's rejection be overturned.

SUMMARY

In summary, Appellants respectfully submit that all of the claims on appeal are patentable over the references cited in the Final Office Action, and respectfully request a favorable decision by the Board.

If there are any charges, please charge Deposit Account No. 50-0221.

Respectfully submitted,

Dated: 2/25, 2005



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